Doc Code: AP.PRE.REQ

PTO/SB/33 (07-05)
Approved for use through xx/xx/200x. OMB 0651-00xx
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Filed electronically

Docket Number (Optional)
34282

I hereby certify that this correspondence is being ~~deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)]~~

on April 9, 2007

Signature /Debra D. Marquis/

Typed or printed name Debra D. Marquis

Application Number	Filed
10/802,203	03/17/2004

First Named Inventor: BLAZEK, ROY J.

Art Unit	Examiner
2823	GREEN, Phillip

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- ☐ applicant/inventor.
- ☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- ☒ attorney or agent of record. Registration number 37,874.
- ☐ attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____

/Thomas B. Luebbering/
Signature

Thomas B. Luebbering
Typed or printed name

816-474-9050
Telephone number

April 9, 2007
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

ARGUMENTS ACCOMPANYING APPLICANT'S REQUEST FOR PRE-APPEAL REVIEW

I. Summary of errors in the Examiner's rejections

Independent claim 1 recites a method of creating a monolithic circuit that generally includes the step of printing a circuit component onto an individual layer of substrate. The Examiner rejected this claim under 35 U.S.C. § 102(b) as being anticipated by Rutt (U.S. Patent No. 3,772,748). Rutt discloses screen printing a temporary or heat-removable bond material onto a substrate that creates a void into which conductive material is later infused. The temporary bond material utilized by Rutt cannot be considered the same as the circuit component recited in claim 1 because the temporary bond material does not form a portion of a circuit. Thus, the Examiner failed to demonstrate that claim 1 and all other clams are anticipated by Rutt.

II. Status of the claims

Claims 1-14 are pending with claims 1, 7, 11, and 14 being independent. No claims have been allowed by the Examiner.

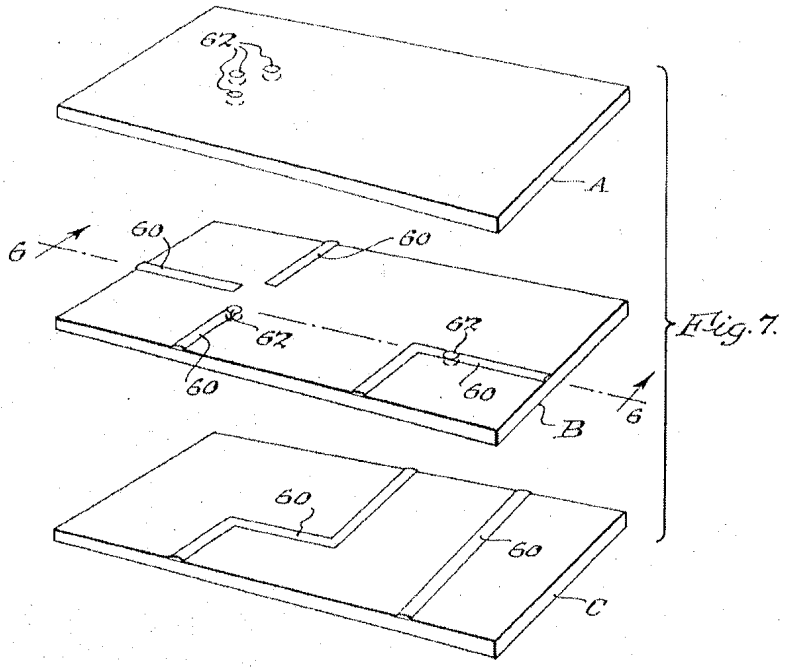
III. Discussion of the claimed method

Independent claim 1 recites a method of creating a monolithic circuit that includes the step of printing a circuit component onto an individual layer of substrate. Claim 7 recites a method of creating a multilayer monolithic circuit that includes the step of printing a circuit component onto an individual layer of thick film ceramic substrate. Claim 11 recites a method of creating a multilayer monolithic circuit that includes the step of screen-printing a plurality of circuit components onto a plurality of individual layers of thick film ceramic substrate. These steps are discussed in the detailed description of the application at least at ¶ 0019. The printed circuit components may be, for example, resistors, inductors, or capacitors.

The method may also include firing the individual layer of substrate, or thick film ceramic substrate, and the circuit component which is printed thereon. The circuit component may be adjusted or trimmed as necessary to achieve some degree of desired precision. Next, a bonding agent may be applied to the individual layer of substrate, or thick film ceramic substrate, and the individual layer of substrate can be assembled with one or more layers of substrate. The method may further include firing the assembled individual layers of substrate and one or more

other layers of substrate together to activate the bonding agent, thereby bonding the individual layer of substrate to the one or more other layers of substrate and creating a multilayer monolithic circuit structure.

IV. Summary of the Examiner's reference



Rutt Figure 7 (Multilayer circuit structure)

Rutt generally discloses a method of creating multilayer circuit structures. Rutt's method begins with creating thin sheets of ceramic dielectric material 25, A, B, C onto which is patterned a temporary fugitive bond material 27, 60 in a desired configuration. The configuration corresponds to the location of targeted capacitor plates 15, or pseudoplates, in the case of the multilayer capacitor of Fig. 1 or to the location of targeted conductive traces 60, or pseudotraces, in the case of the multilayer circuit structure above in Fig. 7. The temporary fugitive bond material does not form the actual capacitor plates or conductive traces, but rather forms *placeholders* for the plates or traces, which are added later, as discussed below. The sheets of ceramic dielectric material with the patterned temporary bond material are stacked in quantities of up to ten and aligned so that the pseudoplates 15 or pseudotraces 60 on one sheet

are registered with the corresponding pseudoplates or pseudotraces 60 on adjacent sheets. The stack is pressed and then cut to form smaller blocks or chips. The chips are heated slowly in air so that the temporary bond material "decomposes", is "driven off", or "burns out". Thus, the temporary bond material, which was patterned, no longer exists and a void, or hole, is left in the place where the fugitive material used to be. The chips are further heated at a higher temperature to sinter the stack. (Discussed in column 3, lines 26-43 and Examples 1-5).

Rutt's process continues by impregnating conductive material into the voids where the temporary bond material used to be. The chips are immersed in a pressurized bath of molten metal, typically silver nitrate, which fills the voids left by the bond material. After a time, the chips are removed and then heated to decompose the silver nitrate, leaving only silver deposits in the voids. These silver deposits form the actual capacitor plates and conductive traces. Termination electrodes or leads may be attached to the exposed conductive material where there are voids. (Discussed in Examples 6-12 and column 12, lines 15-21).

V. The errors in the Examiner's rejections under 35 U.S.C. § 102(b)

A. Rutt does not disclose or suggest printing a circuit component

In the Office Action of January 24, 2007, only once does the Examiner offer a specific location in Rutt to support a portion of his rejection. Otherwise, when attempting to offer support for a claim rejection, the Examiner merely refers to "Figs. 1-7 and related text in Col. 2, line 11 – Col. 14, line 29". Such wholesale designation of the entire specification as a basis for rejection does not satisfy the Examiner's burden under 37 CFR § 1.104(c)(2) to particularly designate the relied-upon portions of Rutt as nearly as practicable. For this reason alone, the Examiner's rejections cannot be sustained.

Further, it is clear that Rutt does not disclose or suggest printing a circuit component as is recited in all independent claims. Instead, the pseudoconductors identified by the Examiner are not circuit components because they are temporary place-holding elements that do not form a portion of any circuit or circuit element.

In particular, the Examiner refers to Fig. 7, as shown above, and states that "individual layers A, B, C contain, structures 60 and 62 are formed using print screen (see Col. 11, line 60 – Col. 12, line 28) and the elements 60 and 62 are also part of circuit components." As discussed in the passage of Rutt to which the Examiner refers, the structures 60 and 62 are "pseudoconductors", "which upon firing to sintering temperature will develop a network of interconnected pores." Therefore, structures 60 and 62 are not circuit components or even "parts of circuit components" as the Examiner states, but rather are short-term placeholders which disintegrate upon heating (Col. 5, lines 10-14). As a temporary place-holding element that disintegrates before a circuit is formed cannot be considered a component of the circuit, the Examiner has failed to demonstrate that Rutt discloses printing a circuit component onto an individual layer of substrate, as is recited in all independent claims of the present application.

B. Rutt does not disclose or suggest firing a substrate layer with a circuit component printed thereon

In the "Response to Arguments" section (Office Action of January 24, 2007), the Examiner states that "Rutt discloses firing of small ceramic units or chips to sinter them into unitary bodies (See Figs. 6 and Col. 11, lines 9-60) which is analogous to 'printing circuit components onto an individual layer substrate; firing the layer of substrate and the circuit component printed there on,' as recited in claims 1, 7 and 11."

Rutt does disclose firing of small ceramic units. However, instead of firing a layer of substrate with the circuit component printed thereon, as recited in claims 1, 7, and 11, Rutt discloses firing layers of substrate including only the temporary bond material (See Example 1). As established above, the temporary bond material is not a circuit component and is disintegrated before the formation of any circuit. Hence, firing layers of substrate and the temporary bond material thereon is not analogous to firing a layer of substrate with a circuit component printed thereon as recited in the independent claims.

C. Rutt does not disclose or suggest adjusting a printed circuit component

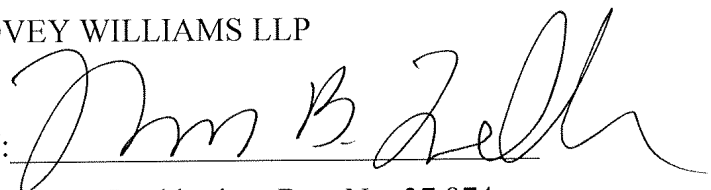
The method of claims 1, 7, and 11 includes the step of adjusting the circuit component as necessary to achieve a desired degree of precision. The Examiner makes no reference whatsoever to any passage in Rutt that discloses this step. Indeed, Rutt does not disclose or suggest the step of adjusting the circuit component as necessary because Rutt does not disclose printing circuit components onto layers of substrate that can be adjusted. The printed temporary bond material does not require any adjustment before heating and disintegrates after heating. The infused metal is buried within layers of ceramic material and cannot be accessed to be adjusted. Thus, since the Examiner fails to make any argument supporting a rejection of this step of the claimed methods, and Rutt does not disclose or suggest this step, the Examiner's rejections of claims 1, 7, and 11, cannot stand.

VI. Conclusion

In view of the foregoing, Applicant respectfully submits that the Examiner has failed to demonstrate that the claims of the current application are anticipated or rendered obvious by the prior art reference Rutt. Should any questions remain, please contact the undersigned. Any additional fee which might be due in connection with this application should be applied against our Deposit Account No. 19-0522.

Respectfully submitted,

HOVEY WILLIAMS LLP

BY: 

Thomas B. Luebbering, Reg. No. 37,874
2405 Grand Blvd., Suite 400
Kansas City, Missouri 64108
(816) 474-9050

ATTORNEYS FOR APPLICANTS